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The People's Processor

Microsemi Rolls Out "Mi-V" RISC-V Ecosystem

by Kevin Morris

The capitalist computing bourgeoisie want to enslave us all with proprietary processing architectures, but the proletariat eventually produces its own processor alternative – an ISA for and by the people, where instruction aren't subject to the whim of the royalty-driven class, and where licensing fees don't oppress the workers' BOM RISC-V is that ISA – the people's processor, the unmoving, unwavering instruction set whose implementation carries no fees or encumbrances, whose workings are left to the needs of the engineer, and whose performance isn't controlled by or limited b ruling class.

The RISC-V revolution won't be televised, however. The proletariat just doesn't have the budget for that sort of thing, so we'll do our best to br you the news right here. With ARM Tech Con – an annual celebration of proprietary processor IP and ecosystems – upon us, we'll take a mor to look at one of the emerging alternatives, on the heels of Microsemi's announcement of a new RISC-V ecosystem for the company's FPGA offerings. Now, a for-profit company offering an "ecosystem" for an open-source ISA may seem more "Red Hat" than "Red Square," but the benefits of an open-source processor can be realized only if there are practical ways that everyday engineers can use them in their designs.

RISC-V is is a standard open-architecture ISA under the governance of the RISC-V Foundation. RISC-V aims to provide portability between silic platforms, so software written to run on a soft core in an FPGA, for example, could easily work in a subsequent ASIC implementation – even a different processor implementation of the RISC-V ISA. The open source approach is intended to allow the broad community to evolve proce IP cores at a faster pace than closed ISAs. Also, since the RISC-V IP core is not encrypted, it can be examined and modified, which enables certifications not possible with closed architectures.

Microsemi has long been involved in providing soft-core processors for use in their low-power, high-reliability FPGA families (which came fro Microsemi's acquisition of Actel several years back). The company offers both RISC-V and ARM-based MCU IP – with the royalty for the ARM cores factored into the price of certain devices. RISC-V enables a more straightforward and portable approach, however, if your team is inclin take a peek outside the normal comfort and security of the well-traveled ARM universe. The Mi-V ecosystem is designed to facilitate just that

Microsemi says that the new Mi-V ecosystem "brings together a number of industry leaders involved in the development of RISC-V to leverag their capabilities and streamline RISC-V designs for customers." Microsemi's PolarFire, RTG4, SmartFusion2 and IGLOO2 field programmable array families all support RISC-V processor IP cores. The company's original RISC-V core clocked in at 2.01 CoreMark and occupied about 10 LUTs. Microsemi has just announced a new, second RISC-V soft core that adds support for single-precision floating point to bolster their line The floating-point version occupies 26K LUTs. There is also a super-minimal 4K LUT version on the drawing board – scheduled for release in 2018.

Microsemi claims that at 2.01 CoreMark/MHz, their RISC-V outperforms other soft-core processors on the market, including the ARM Cortex M MicroBlaze, and NIOS II/EF. Performance is only a small part of the picture, though, since RISC-V could be implemented in just about any FPG and the other options are all either commercially licensed or completely proprietary to one FPGA vendor. Clearly the big attraction of RISC-V is openness.

The Mi-V ecosystem includes the SoftConsole Eclipse IDE, which is common across Microsemi's ARM and RISC-V offerings, allowing a singl debug environment and easy portability of software between the two processor architectures. SoftConsole runs on Linux or Windows, and it i bundled with example projects and RTOSs. There is also a firmware catalog with fully-supported, version controlled, MISRA/Netrino-compliai drivers – complete with release notes and user guides. See, we're getting away from that open-source stigma already.

Regarding RTOS/OS support – on the open-source side, we've got FreeRTOS, Huawei LiteOS, and MyNewt. If you'd rather have commercial support with the RTOS for your open-source processor, you might prefer ExpressLogic's ThreadX, or SiLabs Micrium µC/OSIII. All of them sup the Mi-V RISC-V ecosystem.

There are also some starter design examples targeted to various development boards, including Hello world printf via UART, Interrupt blinky, Touch screen Tic-tac-toe, and a Crypto processor with RISC-V – all available on Github, along with a tutorial called "getting started building a RISC-V" and a "RISC-V Hardware Abstraction Layer to port from ARM Cortex-M." These resources should provide a good jumping-off point fo getting a RISC-V implementaion up and running the first time, or for porting an application from an ARM Cortex-based implementation.

As one might expect, there are several development boards that support the Mi-V RISC-V ecosystem. Microsemi offers one for each of their F families – PolarFire evaluation kit, RTG4 Development kit, and Mi-V IGLOO2 Creative Development Board from Microsemi, as well as the HiFi FE310 Arduino Platform from SiFive's "Freedom Unleashed Platforms." Each of these boards is compatible with the Mi-V ecosystem, and sev more boards are reported to be on the way.

RISC-V offers a solid, viable option for design teams who want to take advantage of the portability, lack of royalties, frozen instruction set, ar flexibility in the processor architecture itself. For many applications, these are attributes form a uniquely compelling proposition. Microsemi's brings solid commercial support to RISC-V, which may well be the final tipping point for many commercial projects. It will be interesting to wa

2 thoughts on "The People's Processor"

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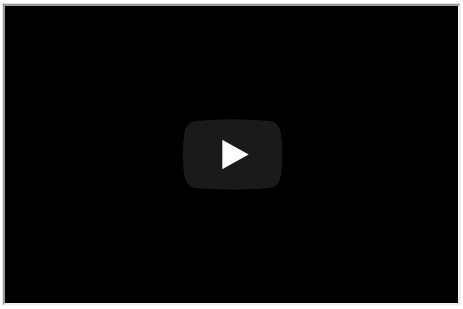

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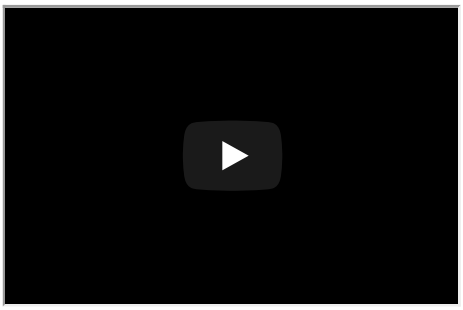

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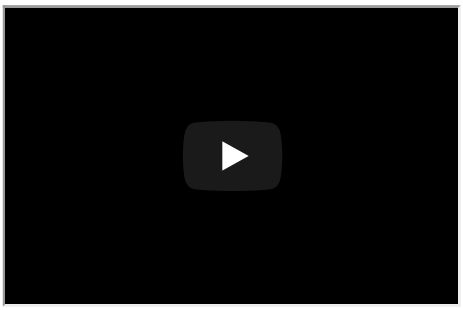

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